generated from minute static electricity occurring around a circuit. There is continuous generation of static electricity when a human body makes movement, and the human body acts as a carrier that carries a great amount of charge. Therefore, if the human body comes close to a conductor, the static electricity is discharged, causing a great amount of current to flow within a short time. Thus, as the amount of charge required to damage a transistor is very small, an ESD protection circuit 2 is provided to an input pin between a pad 1 and a main chip 3 so that the static electricity, rushing into an inner part of the main chip 3, is discharged through an appropriate circuit for maintaining voltages on an input terminal and an output terminal within fixed ranges. Thus, an input protection circuit and an output protection circuit are required for prevention of static breakdown.

Please replace the paragraph beginning on page 2, line 23, with the following rewritten paragraph:

--Referring to Fig. 2, the first exemplary related art ESD protection circuit is provided with a plurality of first transistors 11 each having a collector connected to an input pin between a pad 1 and a main chip 3, and a gate and an emitter both grounded, wherein a voltage from the pad 1 is provided to the main chip 3 directly in a regular case and an inflow of a static electricity is bypassed to the transistors 11, thereby protecting the main chip 3.--

Please replace the paragraph beginning on page 3, line 5, with the following rewritten paragraph:

--Referring to Fig. 3, the second exemplary related art ESD protection circuit is provided with a plurality of second transistors 12 each having a collector connected to an input pin between a pad 1 and a main chip 3 through a first resistor 13, a gate grounded, and an emitter grounded through a second resistor 14, wherein a voltage from the pad 1 is provided to the main chip 3 directly in a regular case and an inflow of static electricity is bypassed to the transistors 12, thereby protecting the main chip 3.~~.~~

B2

Please replace the paragraph beginning on page 3, line 13, with the following rewritten paragraph:

~~--~~First, the related art ESD protection circuit, having the plurality of transistors each with the collector connected to the input pin between the pad and the main chip and the gate and the emitter both grounded, i.e., no resistor is connected to the emitter/collector, may be subject to breakage at a particular point caused by momentary concentration of a charge on the particular point in a case of a BJT of single or plural units or in case the static electricity is generated from inside, and a space of the ESD protection circuit for preventing such an occurrence requires a larger area.~~--~~

B3

Please replace the paragraph beginning on page 3, line 20, with the following rewritten paragraph:

B3

--Second, the related art ESD protection circuit, having the plurality of transistors each with the collector connected to the input pin between the pad and the main chip through the first resistor, the gate grounded, and the emitter grounded through the second resistor, is involved in reduction of BJT gain caused by the two resistors connected to the emitter /collector and a drop of an ESD capability.--

Please replace the paragraph beginning on page 6, line 18, with the following rewritten paragraph:

B4

--Referring to Fig. 5, the ESD protection circuit of the present invention includes an NMOS transistor 42 formed on a semiconductor substrate 41, a first ILD (InterLayer Dielectric) layer 43 formed on the semiconductor substrate 41 inclusive of the NMOS transistor 42 and having a first contact hole to a drain of the NMOS transistor 42, a buffered layer 44 formed on the ILD layer 43 inclusive of the first contact hole and electrically connected to the drain for acting as a resistor, a second ILD layer 45 formed on the first ILD layer 43 inclusive of the buffered layer 44 and having a second contact hole to the buffered layer 44, and a pad 1 formed on the second ILD layer 45 inclusive of

B4

the second contact hole and electrically connected to the buffered layer 44, for discharging static electricity through the pad 1, the buffered layer 44, the drain of the NMOS transistor 42, and the source of the NMOS transistor 42.

Please replace the paragraph beginning on page 7, line 7, with the following rewritten paragraph:

Referring to Fig. 6a, the method for fabricating an ESD protection circuit in accordance with a preferred embodiment of the present invention starts with forming an NMOS transistor 42 on a semiconductor substrate 41. As shown in Fig. 6b, a first ILD layer 42 and a first photoresist film are formed

B5

on the semiconductor substrate 41 inclusive of the NMOS transistor 43, and subjected to selective exposure and development to remove only a portion of the first photoresist film in which a first contact hole to a drain of the NMOS transistor 42 is to be formed. The selectively exposed and developed first photoresist film is used as a mask in etching the first ILD layer selectively, to form a first contact hole, and, then, the first photoresist film is removed. Polysilicon and a second photoresist film are formed on the first ILD layer 43 inclusive of the first contact hole, and the second photoresist film is subjected to selective exposure and development to leave the second photoresist film only on a region on which a buffered layer is to be formed. In this instance, instead of the polysilicon, a silicide may be used. The selectively exposed and developed

second photoresist film is used as a mask in etching the polysilicon selectively, to form a buffered layer 44, and, then, the second photoresist film is removed. As shown in Fig. 6c, a second ILD layer 45 and a third photoresist film are formed on the first ILD layer 43 inclusive of the buffered layer 44, and the third photoresist film is subjected to selective exposure and development to remove a portion of the third photoresist film in which a second contact hole to the buffered layer 44 is to be formed. The selectively exposed and developed third photoresist film is used as a mask in selective etching of the second ILD layer 45, to form a second contact hole, and, then, the third photoresist film is removed. Then, a pad 1 is formed on the second ILD layer 45 inclusive of the second contact hole.

B5

Please replace the paragraph beginning on page 8, line 5, with the following rewritten paragraph:

Because the ESD protection circuit of the present invention has a plurality of transistors each with a collector only connected to an input terminal through a resistor, connected to an input pin between a pad and a main chip, and a gate and an emitter both grounded, the ESD protection circuit and the method for fabricating the same is favorable for use in a fast speed device which should have a small input capacitor, because the resistor at the input terminal increases a secondary breakdown voltage and distributes

B6